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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,723	03/03/2004	Joo Ho Lee	2336-247	2626

7590 06/15/2005

LOWE HAUPTMAN GILMAN & BERNER, LLP  
1700 Diagonal Road, Suite 310  
Alexandria, VA 22314

EXAMINER

ABRAHAM, FETSUM

ART UNIT PAPER NUMBER

2826

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/790,723

Applicant(s)

LEE ET AL.

Examiner

Fetsum Abraham

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) the rest is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

The election of claims 1-10 as response to the restriction imposed in the first action has been acknowledged and the argument that the non-elected claims could be examined with out additional examination burden considered. However, method claims are not similar to device claims where the final product only materializes. Each step has to be examined in order as presented. The steps in claims 10-13 are typical examples of additional examination burden imposed if the restriction was lifted. Therefore, the method claims indeed create a different examination environment in contrast to the device claims in the application and the restriction. In view of the discussion above, the non-elected claims have been withdrawn from consideration.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5,7, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,144,412) in view of Gan et al (6,777,263).

Chang et al disclose a wafer level package in fig. 3E comprising a lower micro cap tape assembly carrying a microchip (82) on the upper surface, via connectors (26) through the assembly bonded to the chip by leads (88) on the upper surface and extending to the opposite surface and connected to pad like element portions of the connecting conductors and a cup structure formed by another tape and element (90) hermetically insulating and sealing the chip.

The prior art discloses a similar structure but omits to use wafers rather than tapes and bonding pads rather than "leads" in the structure and further omit to utilize bonding pads on the external connection side of the tape. However, the secondary reference shows a wafer type packaging structure having a lower wafer (208) having a device (204), bonding pads (207) formed at one surface of the wafer connected with the device, a via through the wafer and conductors in the via connected to the pads and extending to the opposite surface of the wafer, external bonding pads (214) on the surface and adapted to be connected to the bonding pads through the via connectors on the opposite surface of the wafer. Clearly each patent discloses an alternate packaging means to the other strictly demonstrating the choice of packaging means available in the art. Gan et al discloses a wafer packaging means whereby the cup like structure handles the wiring elements and the flat substrate as the carrier of the chip and Chang et al discloses the opposite whereby two cup like structures manage the carrier and wiring roles, respectively.

Therefore, it would have been obvious to one skilled in the art to utilize the elements from both structures such that the wafers of the secondary reference replace the tapes in the primary reference, since wafers provide stronger mechanical support. It would further have been obvious to one skilled in the art for the primary reference to use bonding pads on the opposite surface of the carrier tape since the structure provides easier external connections and more stable contact means.

As for claim 2, the cup structure of the primary reference is defined by a cavity at that carries the chip (82).

As for claim 3, the primary reference might have used tape carrier instead of silicon wafer as the cup structure. However, the secondary reference uses a "wafer" in general as the cup like structure. Therefore, it would have been obvious to one skilled to replace the tape cup structure of the primary reference by a silicon wafer from the selection of many elements defined by "wafer" since silicon is the cheapest and most abundant wafer element known in the art.

As for claim 4, the secondary reference teaches about the presence of a sealing member to seal the package (see abstract) and the primary reference also seals the product as shown in the structure and both structures successfully insulate the encapsulated chip by the sealed package.

As for claim 5, figure 12D of the primary reference shows a metal element (21) on the periphery of the chip carrier and a sealing member from one of adhesive or solder ring (metal) (280) on the leads. Metal conductors are formed at the periphery of the chip carrier to simplify electric connection between the external and the chip and a sealant is used to seal the cup structure and the base substrate to secure encapsulation.

As for claim 7, resin is a known adhesive used in the art for its reliability and the primary reference teaches its applicability in column 8, 55-60.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,144,412) in view of Gan et al (6,777,263) and further in view of Sooriakumar et al (5,801,068).

The prior arts might have been silent about anodic bond sealing means in the packaging structures. However, Sooriakumar teaches that such elements are used to hermetically seal microelectronic devices (see column 3, 36-55). Therefore, it would have been obvious to one skilled in the art to use such bonding means in microelectronic packaging structures since the process provides satisfactory sealing with an overall advantage of reduced cost and manufacturing labor (see column 310-12).

Claims 9,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,144,412) in view of Gan et al (6,777,263) and further in view of Nagarajan et al (6,846,725).

The prior arts disclose all subject matters claimed but may have omitted to provide passivation layer to an outer surface of the dry packaging films. However, Nagarajan et al shows a dry wafer packaging structure (352) in the front page provided with a passivation layer (356) on the outer surface. Therefore, it would have been obvious to one skilled in the art to provide such films to dry packaging structures in general and the prior arts in particular since the additional layer provides the packages with additional mechanical strength and insulation advantages.

As for claim 10, passivation layers such as resins, polymers, oxides and nitrides among the known elements in the art are exchangeable. In this particular case, it would have been obvious to one skilled in the art to use resins or other polymers rather than the oxide material in the structure of Nagarajan et al since such materials are stronger

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than oxides, thereby providing a stronger mechanical support to packaging structures overall.

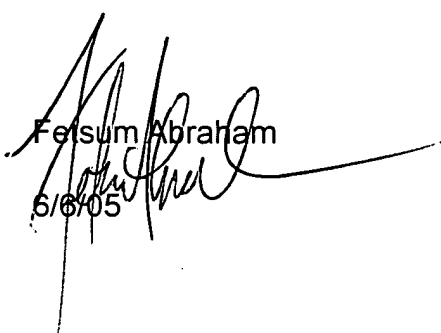
Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The claimed glass frit sealant material for the claimed package and a passivation layer of the claimed type on the outer surface of said dry film structure in the particularly claimed packaging arrangement are not taught or rendered obvious by the prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham  
6/6/05

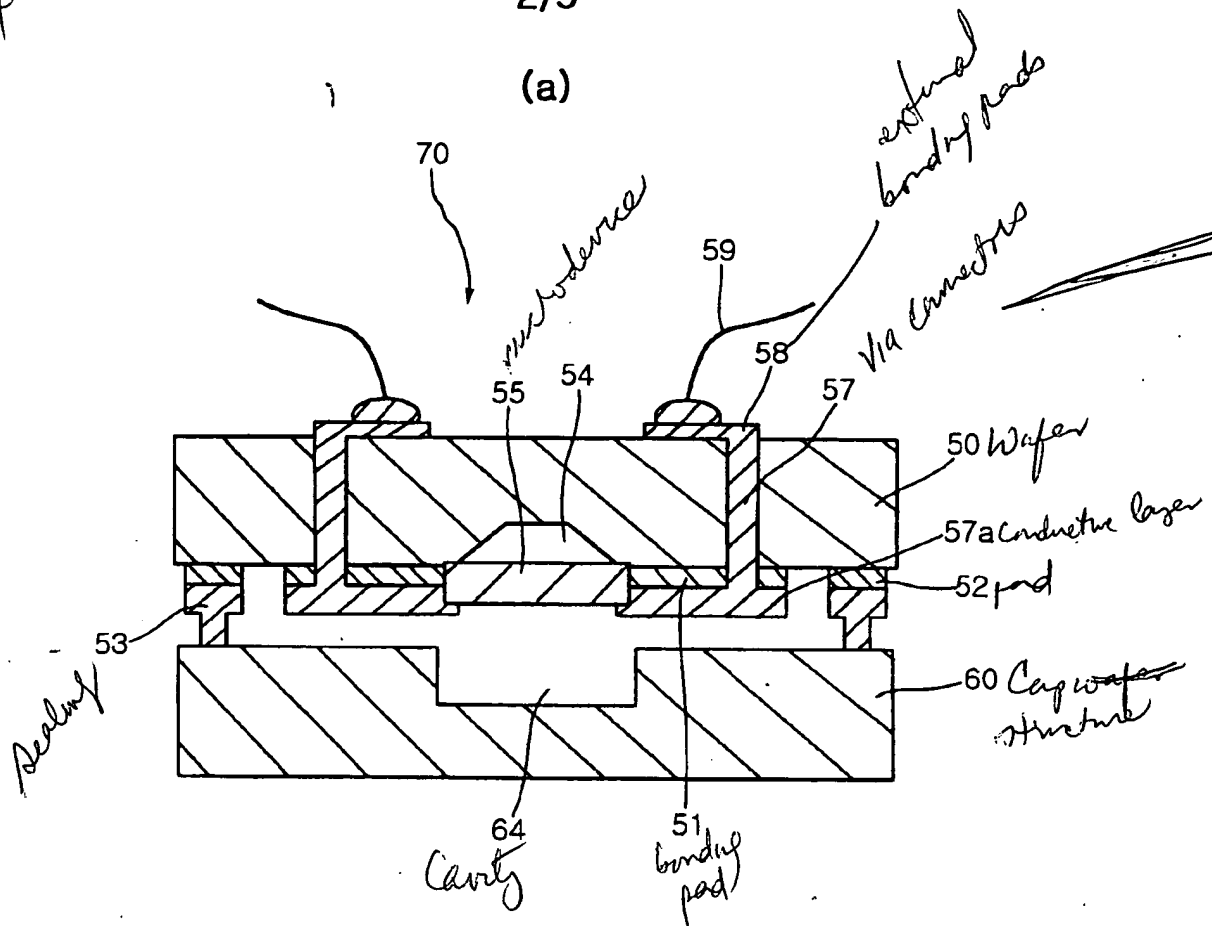


WAFER LEVEL PACKAGE FOR MICRO DEVICE AND MANUFACTURING METHOD  
THEREOF

Inventor: Joo Ho LEE  
Docket No. 2336-248

2/5

(a)



(b)

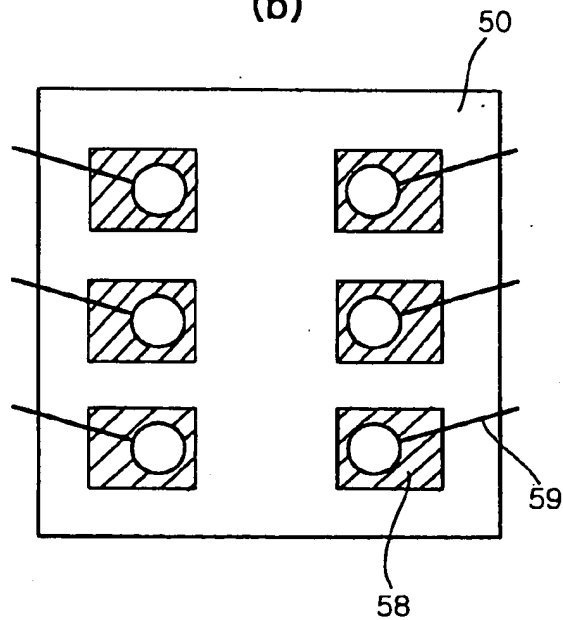


FIG. 3